REMARKS

The Office Action dated October 5, 2004 has been received and carefully noted. The following remarks are submitted as a full and complete response thereto.

In accordance with the foregoing, claims 56, 58, 81, 82, 85, and 90 have been amended. No new matter is being presented, and approval and entry are respectfully requested.

Claims 56-81 and 84 have been allowed, claims 50-52, 88, and 89 are objected to as being dependent upon a rejected base claim, but would allowable if rewritten in independent form including all of the recitations of the base claim and any intervening claims. Claims 48, 49, 53-55, 82, 83, 85-87, and 90 stand rejected. Claims 48-90 are pending and under consideration.

OBJECTIONS TO SPECIFICATION AND CLAIMS:

In the Office Action, at page 2, the Specification and claims 56 and 58 are objected to for minor informalities. The Specification and claims 56 and 58 are amended herein, taking the comments in the Office Action into consideration and directed to overcoming the objections thereto. The Applicant respectfully requests that the Examiner withdraw the objections thereto.

REJECTION UNDER 35 U.S.C. § 112:

In the Office Action, at page 2, claims 82, 83, 85, and 90 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

In response, the claims have been amended to improve clarity and, thereby, in compliance with 35 U.S.C. § 112, second paragraph.

Accordingly, it is respectfully requested that the 35 U.S.C. § 112, second paragraph, rejections of the claims be withdrawn.

REJECTION UNDER 35 U.S.C. § 102:

In the Office Action, at page 2, claims 48, 53-55, and 86 are rejected under 35 U.S.C. § 102 as being anticipated by U.S. Patent No. 6,194,962 to Chen ("Chen '962"). The Office Action took the position that Chen '962 describes all the recitations of claims 48, 53-55, and 86. This rejection is traversed and reconsideration is requested.

Independent claim 48, upon which claims 48-55 are dependent, recites a wide input range amplifier including a first and second stage. The a first stage having first and second inputs, first and second outputs, and first, second and third voltage sources, outputting a first output signal being amplified a first amount. A second stage has first and second inputs connected to the first and second outputs of the first stage, respectively, and accepts input signals and outputting a second output signal being amplified a second amount. The first stage includes two input stages, the two input stages including a first input stage of a first conductive type and a second input stage of a second conductive type.

Independent claim 82, upon which claims 83 and 85 are dependent, recites a method for receiving a signal. The method includes receiving a thick device signal, amplifying the thick device signal a first amount and stepping the thick device signal down to a first thin device signal, and amplifying the first thin device signal a second amount and outputting a second thin device signal. The amplifying of the first thin device signal includes adjusting a gain of the differential transistors to produce the second thin device signal as a differential output.

Independent claim 86, upon which claims 87-90 are dependent, recites a wide input range amplifier including a first amplifying means for accepting input signals and

outputting a first output signal being amplified a first amount, and a second amplifying means for accepting input signals and outputting a second output signal being amplified a second amount. The first amplifying means includes a first input stage of a first conductive type and a second input stage of a second conductive type.

As will be discussed below, the cited prior art of Chen '962 fails to disclose or suggest the elements of any of the presently pending claims.

Chen '962 generally describes an op amp with adaptive offset voltage as shown in FIG. 4. See column 4, lines 64-67. The amplifier has an input stage 28 which includes a first differential pair MP1 and MP2 (referred to herein as "MP1/MP2") and a complementary second differential pair MN1 and MN2 ("MN1/MN2"). See column 3, lines 46-64. MP1/MP2 are biased with respect to the amplifier's positive supply voltage VDD, and MN1/MN2 are biased with respect to the amplifier's negative supply voltage VSS, providing a common-mode input voltage range that includes VDD and VSS (i.e., a "rail-to-rail" common-mode input voltage range). A current source 30 is connected between VDD and the source terminals of MP1/MP2 and provides a bias current I_{bias} to the pair. MN1/MN2 are biased via a "switching/current sense" circuit 32 connected between the source terminals of MN1/MN2 and VSS. Switching/current sense circuit 32 is preferably implemented with a pair of transistors MP3 and MP4, which have their gates commonly connected to a reference voltage Vref. See column 5, lines 16-18.

On the bottom of page 2 of the Office Action, it is contended that the arrangement of MP1, MP2, MN1, and MN2 may be read as the first stage claimed in independent claim 48. The Office Action further contends that VDD, VSS, and Vref of Chen '962 may be construed to read on the first, second, and third voltage sources recited in independent claim 48. Applicants respectfully disagree. Vref of Chen '962 cannot be construed to be the same as the third voltage source recited in independent claim 48 because Vref is not part of the MP1, MP2, MN1, and MN2 arrangement, which the Office Action has read as the first stage claimed in independent claim 48. Rather, Vref is connected to the switching/current sense circuit 32, which is preferably implemented with

a pair of transistors MP3 and MP4, which have their gates commonly connected to the reference voltage Vref.

Independent claim 48 clearly recites "wide input range amplifier comprising: **a first stage having** first and second inputs, first and second outputs, and first, second and **third voltage sources**, outputting a first output signal being amplified a first amount; a second stage having first and second inputs connected to said first and second outputs of said first stage, respectively, said second stage accepting input signals and outputting a second output signal being amplified a second amount, wherein said first stage includes two input stages, said two input stages including a first input stage of a first conductive type and a second input stage of a second conductive type." Emphasis added. Thus, Applicants respectfully assert that it is improper to construe the MP1, MP2, MN1, and MN2 arrangement as the first stage and then construe the voltage source Vref, which is included in a different arrangement (i.e., the switching/current sense circuit 32), as the third voltage source recited in independent claim 48.

In addition, referring to Chen '962, MP1/MP2 is biased with current source 30. MP1/MP2's differential output current I_{outp} is connected to output stage 34, which is implemented as a folded cascode stage into which I_{outp} is summed. MN1/MN2's differential output current I_{outn} is mirrored by current mirrors 40 and 42 and summed into the folded cascode stage. See column 4, line 65, to column 5, line 7. Output stage 34 converts the summed differential output currents I_{outp} and I_{outn} to single-ended amplifier output I_{out}.

The Office Action contends that the MP1, MP2, MN1, and MN2 arrangement is the first stage and the output stage 34 is the second stage. As shown in FIG. 4 of Chen '962, the differential output currents I_{outp} and I_{outn}, from MP1/MP2 and MN1/MN2 (i.e., the first stage) and the current mirrors 40 and 42, respectively, are provided to the output stage 34 (i.e., the second stage) as bias currents, which are then converted to the single-ended output I_{out}.

In contrast, independent claim 48 recites, "a second stage having first and second inputs connected to said first and second outputs of said first stage, respectively." The first and second inputs of the output stage 34 in Chen '962 are not connected to the first and second outputs of the MP1/MP2 and MN1/MN2. As shown in FIG. 4 of Chen '962, the first and the second outputs of the MP1/MP2 and MN1/MN2 are connected to the drain elements of the output stage 34.

Furthermore, referring to independent claims 48 and 86, the output stage 34 converts a sum of the two differential output currents I_{outp} and I_{outn} to a single-ended output I_{out} as the amplifier's output and varies the output I_{out} in accordance with a value of a trim signal received. The trim signal is active only when MN1/MN2 are active and it is not active when MP1/MP2 are active. See column 4, lines 40-43. The trim signal enables the amplifier's input offset voltage V_{os} to be reduced and brought closer to its ideal value of zero. See column 4, lines 5-8. However, Chen '962 does not teach or suggest that the output stage 34 accepts I_{outp} and I_{outn} and outputs "a second output signal being amplified a second amount," as recited in independent claims 48 and 86.

Accordingly, it is respectfully asserted that Chen '962 fails to teach or suggest all the recitations of independent claims 48 and 86 and related dependent claims.

In the Office Action, at page 3, claims 86 and 87 are rejected under 35 U.S.C. § 102 in view of U.S. Patent No. 6,5,734,297 to Huijsing et al. (Huijsing '297). The Office Action took the position that Huijsing '297describes all the recitations of claims 86 and 87. This rejection is traversed and reconsideration is requested.

According to the Office Action, the arguments presented in response to the Office Action of July 9, 2004 supporting the patentability of claims 86 and 87 in view of Huijsing '297 are not clear. Those arguments will be clarified as set forth below.

In the Office Action of July 9, 2004, it was contended that, in FIG. 5b of Huijsing '297, Q1-Q4 represent complementary input pairs that are analogous to the first and

second input stages of the first amplifying means recited in claims 86 and 87 of the present application. It was also contended that elements Q11-Q14 represent cascade transistors that are analogous to the second amplifying means recited in claims 86-87.

However, as shown in FIG. 5b of Huijsing, elements Q1 and Q3 are PNP switches and Q2 and Q4 are NPN switches. Thus, if, as construed by the Office Action, elements Q1-Q4 are construed to be the first amplifying means recited in independent claim 86, elements Q1-Q4 are not "of a first conductive type," as recited in independent claim 86. Rather, elements Q1-Q4 include at least two elements being NPN and the other elements being PNP elements. Thus, elements Q1-Q4 are of at least two conductive types.

Similarly, as shown in FIG. 5b of Huijsing, elements Q11 and Q13 are NPN switches and Q12 and Q14 are PNP switches. Thus, if, as construed by the Office Action, elements Q11-Q14 are construed to be the second amplifying means recited in independent claim 86, elements Q11-Q14 are not "of a second conductive type," as recited in independent claim 86. Rather, elements Q11-Q14 include at least two elements being NPN and the other elements being PNP elements. Thus, elements Q11-Q14 are of a first conductive type and a second conductive type.

Thus, elements Q1-Q4 appear to be described in Huijsing '297 as being of a first conductive type (e.g., N) and of a second conductive type (e.g., P). Similarly, elements Q11-Q14 appear to be described in Huijsing '297 as being of a first conductive type (e.g., N) and of a second conductive type (e.g., P). Therefore, elements Q1-Q4 and Q11-Q14 are not of either a "first conductive type" or of a "second conductive type", as are each of the input stages recited in claims 86-87.

Thus, since Huijsing '297 discloses or suggests no other components that are analogous to the first and second amplifying means of the claimed invention, Huijsing '297 fails to disclose or suggest the recitations of independent claim 86 and related dependent claim 87.

REJECTION UNDER 35 U.S.C. § 103:

In the Office Action, at page 4, claims 49 and 87 are rejected under 35 U.S.C. § 103 as being unpatentable over Chen '962. The Office Action took the position that Chen '962 disclosed all the elements of claims 49 and 87, as the trim circuits 36 of Chen '962 are connected across the outputs of the input pairs and would be functionally equivalent to the claimed resistors. The rejection is traversed and reconsideration is requested.

The arguments presented above are incorporated herein to support the patentability of claims 49/48 and 87/86 over Chen '962. Accordingly, it is respectfully asserted that independent claims 48 and 86 and related dependent claims 49 and 87, respectively, are allowable.

CONCLUSION:

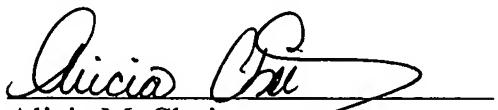
In view of the above, applicant respectfully submits that the claimed invention recites subject matter which is neither disclosed nor suggested in the cited prior art. Applicant further submits that the subject matter is more than sufficient to render the claimed invention unobvious to a person of skill in the art. Applicant therefore respectfully requests that each of claims 45-55, 82, 83, and 85-90 be found allowable, in addition to the allowed claims 56-81 and 84, and this application passed to issue.

If for any reason the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact, by telephone, the applicant's undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper is not being timely filed, the applicant respectfully petitions for an appropriate extension of time.

Any fees for such an extension together with any additional fees may be charged to Counsel's Deposit Account 50-2222.

Respectfully submitted,



Alicia M. Choi
Registration No. 46,621

Customer No. 32294
SQUIRE, SANDERS & DEMPSEY LLP
14TH Floor
8000 Towers Crescent Drive
Tysons Corner, Virginia 22182-2700
Telephone: 703-720-7800
Fax: 703-720-7802
AMC